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Fuzzy Logic Controller based Hybrid MMC for DC Fault Current Mitigation in HVDC Grid.

GUNUPATI HYMAVATHI

Student, Dept Of Electrical And Electronics Engineering, Quba College Of Engineering And Technology, Venkatachalam,Nellore,A.P., India

SK SEEMA

Assistant Professor, Dept Of Electrical And Electronics Engineering, Quba College Of Engineering And Technology, Venkatachalam,Nellore,A.P., India

Abstract **– This paper proposes a source-side DC deficiency current leeway plot for HVDC lattices under DC impede. The plan utilizes half-connect sub-modules (HBSM) and full-connect sub-modules (FBSMs) based crossover MMC. The DC issue current practices of the HVDC matrix is uncovered as an essential rule for the proposed approach. The extra levels of opportunity for control of cross breed MMC are joined into the HVDC matrix to intrude on the shortcoming current taking care of at the source side. During the flaw ride-through interaction, the receptive force remuneration is kept up. The proposed technique needn't bother with the DC circuit breakers (DCCBs) since the current in the separation point can be controlled to nothing. The essential and reinforcement insurance plans for mixture MMC-HVDC matrix are proposed. The viability of the technique is approved by electromagnetic transient reproductions on Matlab/Simulink.**

Keywords **– Fuzzy Logic, HVDC Grid, Mitigation, DC Current, Hybrid MMC.**

I. INTRODUCTION

HIGH voltage direct current (HVDC) matrices are drawing in significant considerations because of the expanding interest for enormous environmentally friendly power sources and the fast improvement of promising advances, for example, particular staggered converter (MMC) [1]-[3]. The HVDC framework is viewed as one of the fasible answers for moving huge measure of energies from the fluctuating environmentally friendly power sources over significant distances [4]-[7]. Subsequently, HVDC matrix will have better possibility in designing because of the utilization of overhead line (OHL) for power transmission. One such plan at present under development is the China's four terminal Zhangbei MMC-HVDC lattice project, evaluated at ±500 kV/3000 MW [8]. As an arising new innovation, HVDC lattices are dealing with testing issues, for example, the extreme DC shortcoming ride-through (FRT) [9]-[11]. At the point when DC side shaft to-post short out shortcoming happens, the capacitors in the HVDC matrix converters will take care of flaw flows to the DC lines and may harm the segments in the releasing circuit [12]. The half and half MMC utilized in this paper is appeared in Fig. 1, which is made out of halfbridge sub-modules (HBSM) and full-connect sub-modules (FBSM). Utilizing the negative voltage yield capacity of FBSMs, the DC voltage of half and half MMC can be controlled inside a huge reach, in this way expanding the control levels of opportunities for cross breed MMC.

Concerning the crossover MMC appeared in Fig. 1, there are a few control habits to accomplish the DC flaw ride-through in the references. They are grouped into two classes. In the principal classification, the FRT is accomplished by essentially impeding all the valves in the cross breed MMC. This is the easiest methodology and empowers quick interference of the DC flaw current. Notwithstanding, the mixture converter becomes wild once all the valves are killed, at that point the genuine and responsive Force transmission are intruded. In the event that an enormous scope wind ranches were persistently taking care of capacity to the HVDC framework before the shortcoming, the overvoltage marvel because of the valve hindering may harm the DC overhead transmission lines.

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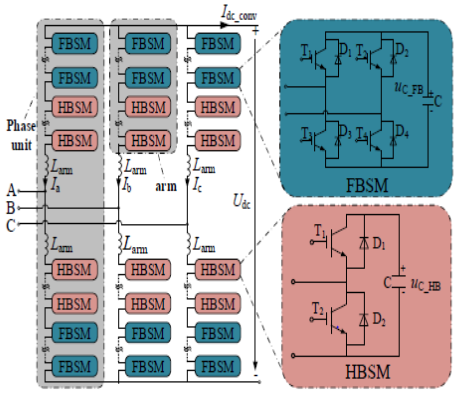

Fig. 1 The structures of hybrid MMC and its submodule topologies.

In the second classification, the FRT cycle is accomplished by changing the basic mode segment of the half breed MMC arm voltage reference to make the DC transport voltages practically equivalent to the leftover voltage of the shortcoming point so the releasing of the MMC capacitors can be halted and the separation point can be detached under zero flows. Notwithstanding, this procedure is more relevant direct to-point HVDC framework where the force transmission will unavoidably be totally intruded. Taking into account that quick releasing of the capacitors in numerous MMCs are firmly coupled, the previously mentioned commonmode control approach is not, at this point relevant, since in any case the genuine force of the whole HVDC matrix will be interfered.

II.SOURCE-SIDE FAULT CLEARANCE OF HYBRID MMCHVDC GRID

In MMC-HVDC lattices, the converters are the primary flaw current taking care of sources under strong shaft to-post short out deficiency. In this brief timeframe scale, the flaw current from the air conditioner side source can be disregarded and the MMC can be addressed by rearranged RLC circuit [11]. The quick current rising is practically wild from the source-side because of the freewheeling diodes in the customary half-connect MMCs. Nonetheless, this isn't the situation for the mixture MMCs.

A. DC Fault Current Contribution Analysis

Expect a four-terminal monopole HVDC matrix utilizing cross breed MMC, as demonstrated in Fig. 2. All control modes and nitty gritty boundaries of converters are given in the index. Note that the proposed control strategy in this paper is similarly relevant to the bipolar HVDC network. In Fig. 2, I1 is the converter current from Station 1 (characterized as Main Feeding Current (MFC)), I31 is the current taking care of from adjoining line (characterized as Auxiliary Feeding Current (AFC)), and I12 is the current of the DC separation point.

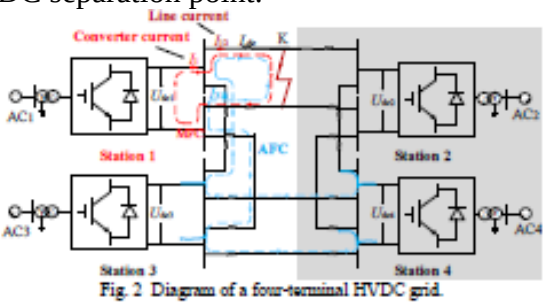

Fig. 2 Diagram of a four-terminal HVDC grid.

At time t = 1.50s, a perpetual shaft to-post flaw happens at area K of the DC line between Stations 1 and 2.

III.CONTROL APPROACH OF HYBRID MMC SUITABLE FOR HVDC GRID

This part means to discover attainable control targets for the mixture MMCs which can interfere with the source-side current taking care of to the HVDC framework, and afterward propose reasonable control systems to accomplish the control goals.

A. Candidate Control Objectives

In Fig. 2, the flaw current taking care of segments of the line current I12 is examined by investigating the deficiency area K from Station 1, at that point the control targets are talked about beneath. To smother the shortcoming current I12, there are two applicant control destinations:

1) Reducing the taking care of current I1 (characterized as converter current of the half and half MMC), if all stations decrease their converter flows, the DC

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shortcoming current I12 will lessen to nothing;

2) Making I1 and I31 equivalent and inverse by controlling the half breed MMCs in Station 1 with the goal that I1 and I31 drop each other at the DC transport and afterward I12 will rough to nothing. This control applicant will be principally talked about in the paper.

Both control goals above can be accomplished through converter control, as demonstrated in the source-side plan in Fig 4, consequently it is characterized as DC deficiency current leeway at the sourceside of HVDC lattice.

B. Additional Control Degree of Freedom for Hybrid MMC

Fig. 1 shows the three-stage design of the crossover MMC, contrasting and the half-connect MMC, the extra control level of opportunity got from utilizing the FBSMs is the adaptability of over balance. The air conditioner side stage voltage and stage current ix (x=a, b, c) of MMC can be communicated as [20]:

$$\begin{cases} u_x = U_m \cos \omega t \\ i_x = I_m \cos(\omega t + \varphi_x) \end{cases} \quad (1)$$

Here, Um and Im are individually the air conditioner framework real voltage and current sizes, φx is the point between the voltage and current vectors and ω is the rakish recurrence of the air conditioner framework.

$$U_m = M_{ac} \frac{U_{dcn}}{2} \quad (2)$$

Where, Udcn is the MMC appraised DC voltage, which is planned by the current rating of the IGBTs and the module tally inside each stage arm. Accept an evaluated capacitor voltage Ucn of both HBSMs and FBSMs in the half breed MMC, and the absolute module tally N=NF+NH, in which NF is the FBSM tally and NH is the HBSM check, consequently Udcn=NUcn. Characterize DC voltage balance proportion Mdc (Mdcmin≤Mdc≤1, and Udcmin is the per unit estimation of the permitted least DC voltage), at that point the real DC voltage Udc fulfills:

$$U_{dc} = M_{dc} U_{dcn} \quad (3)$$

Characterize the air conditioner voltage tweak proportion as Mac, at that point: Disregarding the voltage drops across the half breed arm inductors, at that point as indicated by KVL, acquire:

$$\begin{cases} u_{px} = \frac{1}{2} U_{dc} - u_x \\ u_{nx} = \frac{1}{2} U_{dc} + u_x \end{cases} \quad (4)$$

where, upx and unx (x=a, b, c) are the prompt estimations of the upper and lower arm voltages of mixture MMC separately. In appraised working mode, for example at the point when Mdc=1, from (4) the operational voltage scope of mixture MMC arm is as:

$$\frac{U_{dcn}(1-M_{ac})}{2} \le \{u_{px}, u_{nx}\} \le \frac{U_{dcn}(1+M_{ac})}{2} \quad (5)$$

In diminished DC voltage mode, ac framework voltage size ought to be kept up, at that point the activity scope of arm voltages changes to:

$$\frac{U_{dcn}(M_{dc}-M_{ac})}{2} \le \{u_{px}, u_{nx}\} \le \frac{U_{dcn}(M_{dc}+M_{ac})}{2} \quad (6)$$

Brushing (5) and (6), the total scope of mixture MMC arm voltage under given Mac and Mdcmin is as following:

$$\frac{U_{dcn}(M_{dcmin}-M_{ac})}{2} \le \{u_{px}, u_{nx}\} \le \frac{U_{dcn}(1+M_{ac})}{2} \quad (7)$$

At the point when the half breed MMC is requested to yield negative voltages which depends on the NF FBSMs, Mdcmin＜Mac; When the arm is requested to yield positive voltages, to adjust all the capacitor voltages inside a restricted voltage swells, both HBSMs and FBSMs ought to be chosen by the rising request voltage table. Consequently, the necessary FBSM include in every crossover MMC arm is planned by (8):

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$$N_F = \frac{M_{ac} - M_{dcmin}}{2} N \qquad (8)$$

The plan model of the maximum furthest reaches of the over regulation of mixture MMC is given in (8) while the specific worth ought to be resolved by the planned FRT capacity. Since the extra control level of opportunity is gotten from utilizing more FBSMs in the half breed MMC, the ideal plan of the FBSM tally is a tradeoff among cost and controllability. The advantages for the DC FRT of the HVDC lattice will be examined later.

C. Control Approach for Hybrid MMC

For every cross breed MMC in the four-terminal HVDC lattice as demonstrated in Fig. 2, the regulator structure is appeared in Fig. 3. The half breed MMC controls its DC voltage Udc or genuine force Ps or normal sub-module voltage Uc_avg, it likewise directs its own ac side voltage sizes or receptive force. Hence, the old style vector control procedure with decoupled control of d-and q-hub current can be utilized. The flowing current concealment control (CCSC) block and closest level modulator (NLM) can be utilized in the cross breed MMC, as found in Fig. 3.

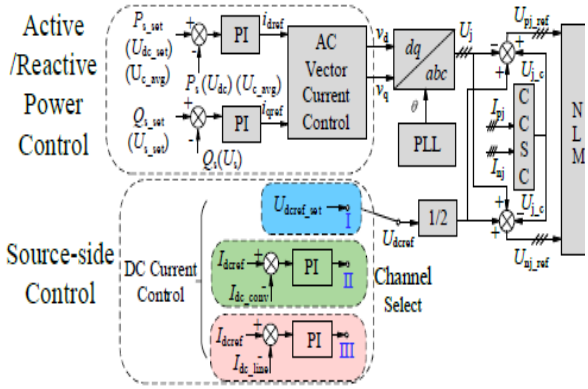

Fig 3 The hybrid MMC block diagram

Fig.3 likewise incorporates the three channels for every cross breed MMC utilized in the HVDC matrix, among which channels II and III have a place with the DC current control mode proposed in this paper. The presentations of the three channels are as per the following and in Section IV we talk about when to pick one of them.

D. The Implementation of the Required DC Voltage Reference in Hybrid MMC

Fig. 4 is utilized to outline how the DC voltage reference is executed in the converter level during the FRT interaction. The arrangement associated FBSMs and HBSMs of a similar stage unit of the converter are controlled to create the ideal half breed arm voltages as indicated by the voltage references Upj_ref and Unj_ref yielded (11).

In Fig. 4, the voltage of the cross breed arm is either sure or negative whenever and there is no voltage scratch-off inside each arm by HBSMs and FBSMs [18]. The DC voltage Udc is the added estimation of the deliberate estimations of the upper and lower arm voltages Upj and Unj (as found in Fig4 and condition (11) gives their reference esteems) and the complete voltage drops across the two arm inductors LARM. The voltage drops across LARM must be by implication constrained by a shut circle way through setting off the FBSMs and HBSMs, and SM states will be resolved utilizing the closest level adjustment (NLM) to control arm voltage as indicated by the references decided from conditions (11-13). The whole voltage of Upj and Unj will follow Udcref and consequently Udc will roughly approach Udcref. The distinction voltage among Udc and shortcoming point voltage (0V) is across the DC reactor LDC, line opposition Rline and line inductance Lline, so the separation point current can be constrained by the converter DC voltage. Fig.4 give the outlines of the MMC circuit

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and the DC current control.

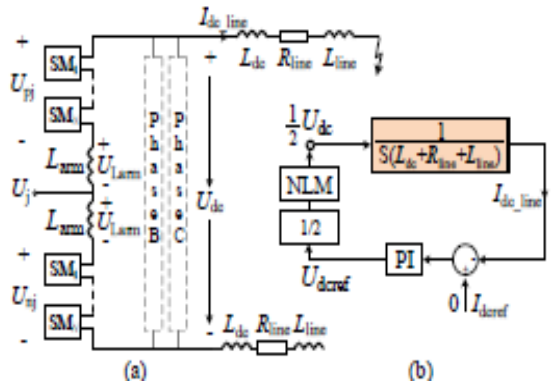

Fig 4 during FRT process the implementation of DC voltage reference

E. DC Fault Ride through Capability Index

The energy scattering in DCCB flood arresters is:

$$E_{DCCB} = \int_0^{t_C} I_{dc}(t) V_{arr}(t) dt \quad (14)$$

Where, Varr is the arrester voltage, Idc is line current and tC is the deficiency current leeway time. With crossover MMC converters, DC voltage can be immediately controlled under DC deficiencies, and the inward current controls will restrict the current sizes. To assess the FRT ability of the DC framework and quantitatively look at the two insurance strategies, a DC Fault Ride-through Capability Index (DC-FRTCI) is proposed here. The base worth is chosen as the flood energy should have been dispersed in the framework without control during the flaw time frame (the relating DC current is Idc), at that point compute the saved energy scattering because of the utilization of the proposed control strategies (the comparing DC issue current is Idc_P), the meaning of the DC-FRTCI list is surrendered (15), and is momentarily delineated in Fig. 7.

$$\text{DC-FRTCI} = 1 - \frac{\int_{t_F}^{t_C} I_{dc\_P}^2(t)\,dt}{\int_{t_F}^{t_C} I_{dc}^2(t)\,dt} \quad (15)$$

IV. Primary and Backup Protection Approach of Hybrid MMC-HVDC Grid

In the MMC-HVDC matrix, a couple of milliseconds (5~6 ms) are accessible for the DCCBs to work after a DC impede. In any case, as expressed in the above control approach, in the half and half MMC based HVDC matrix, the DCCBs are not, at this point required. A mechanical electrical switch (MCB, basically is an AC electrical switch with circular segment breaking ability) can be utilized for flaw detachment, the MCB will activity effectively after flow zero point produced by DC flow control. Consequently the proposed control techniques can be planned into the proposed essential and reinforcement security plot, the stream outline is appeared in Fig. 5.

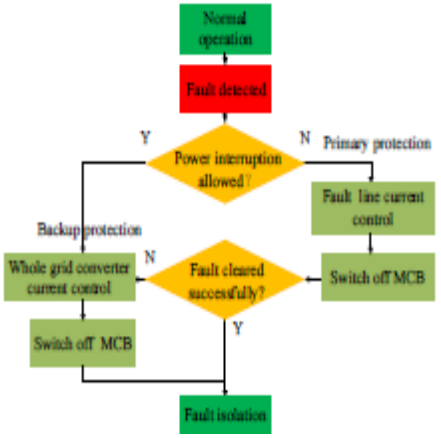

Fig 5 flowchart of protection scheme

At the point when a DC deficiency happens, the capacitors release quick and cause enormous shortcoming flows, thus a rule of the issue discovery is planned by the overcurrent. In Fig. 8, the DC deficiency line current control is characterized as the essential assurance, the converter DC current control of the relative multitude of stations is characterized as a reinforcement security and will be initiated if there should arise an occurrence of undesirable declining activity of the essential insurance of the HVDC network. By and large this is characterized as the planned control technique.

V. Proposed topology with Fuzzy control system:

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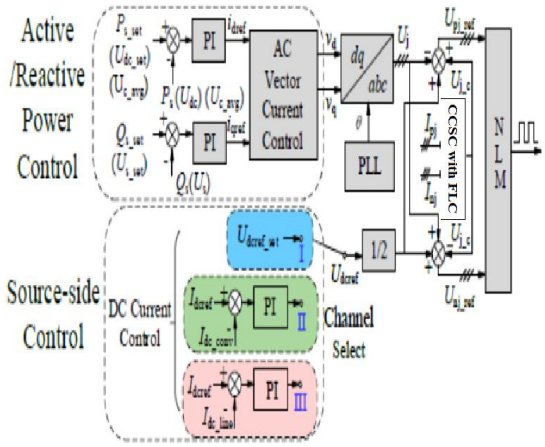


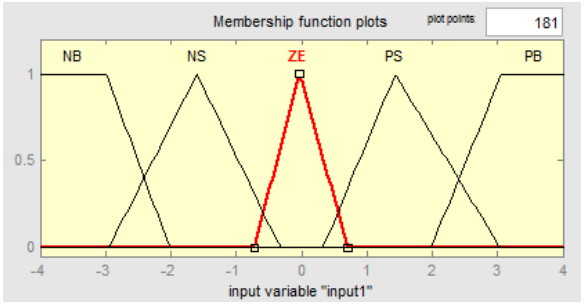
Fig 6 controller diagram with FLC

The proposed toplogy with controller is represented in fig 6.

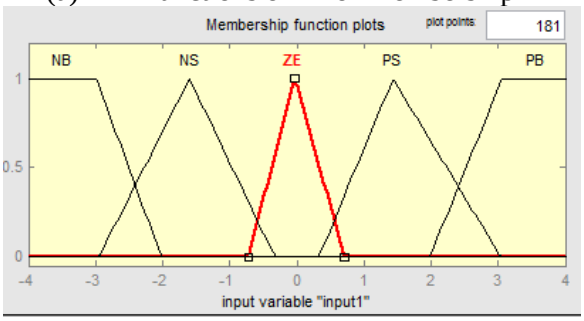
A fuzzy control system is a control structure reliant on fuzzy rationale—a logical structure that examines straightforward information regards similarly as reasonable elements that take on consistent characteristics some place in the scope of 0 and 1, rather than old style or progressed rationale, which deals with discrete assessments of one or the other 1 or 0 (valid or bogus, independently). Fuzzy rationale is extensively used in machine control. The term 'fuzzy' implies the way that the rationale included can oversee thoughts that can't be imparted as the 'valid' or 'bogus' yet rather as part of the way obvious'. Yet elective philosophies, for instance, nonexclusive figurings and neural frameworks can perform comparably similarly as fuzzy rationale a significant part of the time, fuzzy rationale has the favored position that the response for the issue can be tossed in phrasing that human heads can see, so their experience can be used in the design of the regulator. This makes it less difficult to mechanize tasks that are as of now adequately performed by individuals.

a. Fuzzy sets:

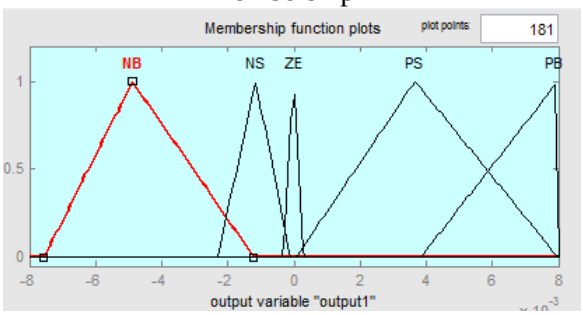
The data factors in a fuzzy control system are all things considered planned by sets of enlistment limits this way, known as fuzzy sets. The route toward changing over a new data motivator to a fuzzy worth is called 'fuzzification'. The enlistment components of the Fuzzy regulator used in our generation model are given as seeks after.



(a) Functions of Error Membership



(b) Functions of Change in Error Membership

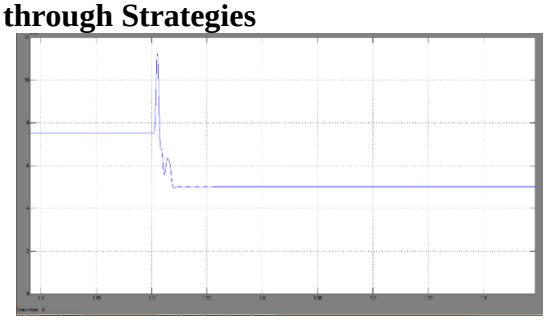


(c) Functions of Output Membership

Fig 7 fuzzy membership functions

VI. Simulation results:

A. Comparison of Control Capability of Non-blocking and Blocking-based Ride-through Strategies



(a) DC fault non-blocking ride through, Reactive power

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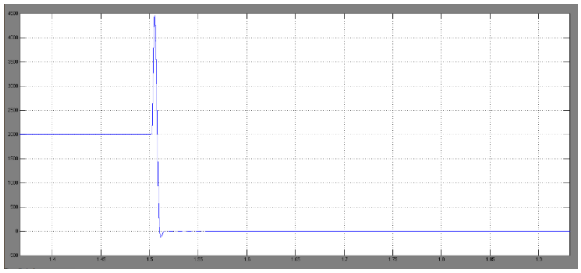
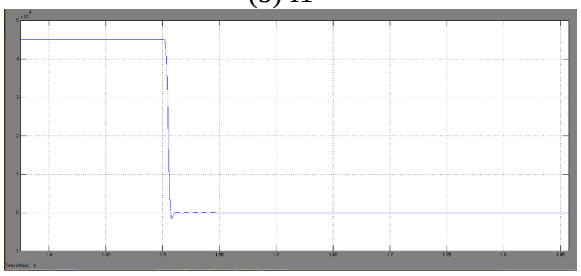
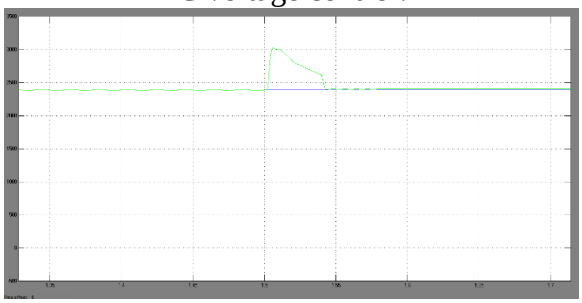


(b) I1

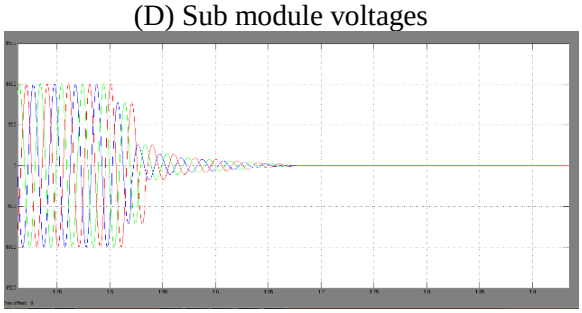


(c) Udc1

Fig. 8 Comparison of reactive power and DC voltage control:

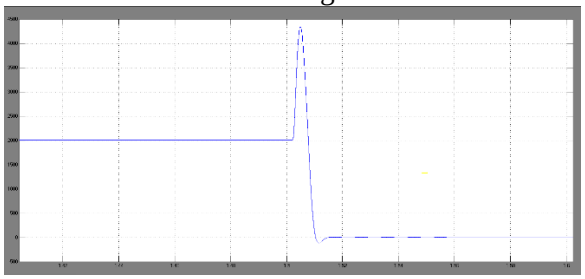


(D) Sub module voltages

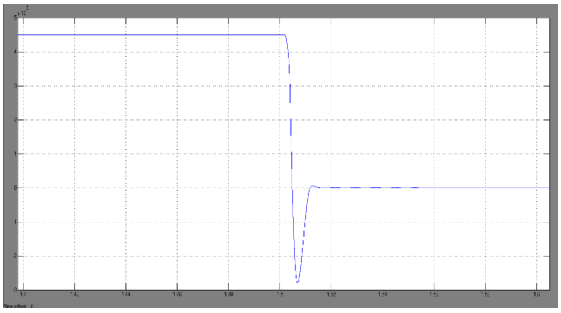


(e) Upper arm current

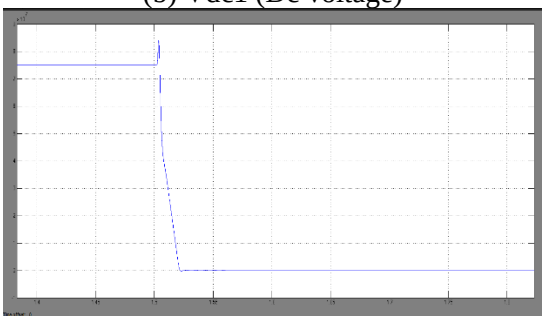
Fig. 9 Comparison of reactive power and DC voltage control: (b) DC fault blocking-based ride through.



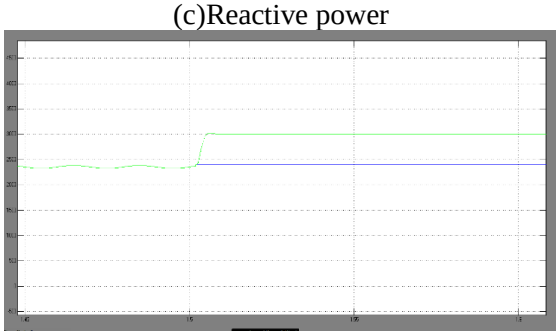
(a) I1



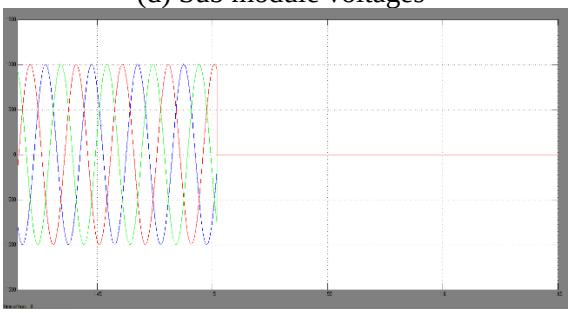
(b) Vdc1 (Dc voltage)



(c)Reactive power

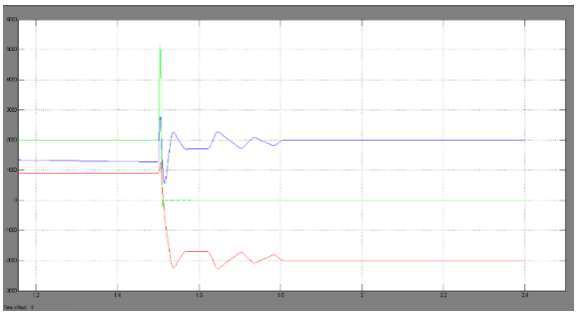


(d) Sub module voltages



(e) Upper arm current

B. Converter DC Current Control Mode



The system transients: (a) DC current

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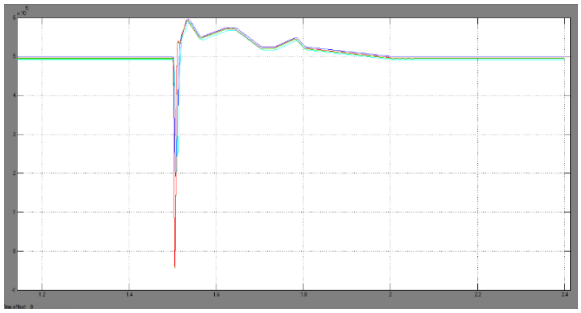
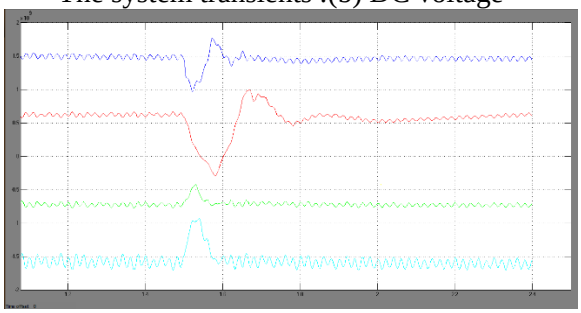
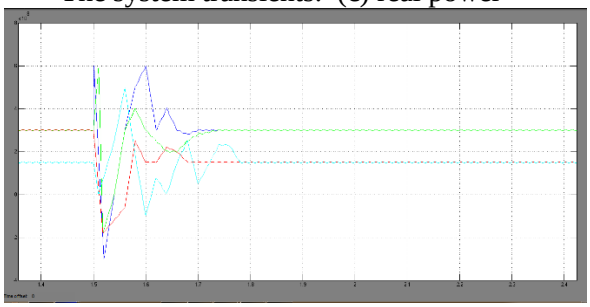


The system transients :(b) DC voltage



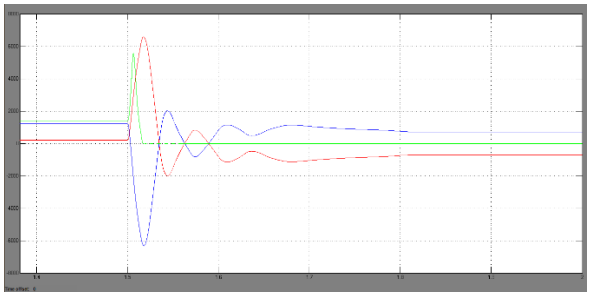
The system transients: (c) real power



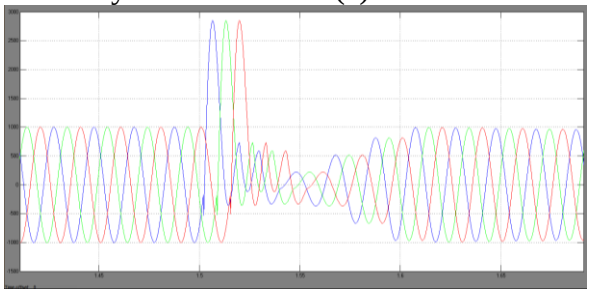
The system transients: (d) reactive power.

Fig. 10 The system transients: (a) DC current, (b) DC voltage, (c) real power, and (d) reactive power.

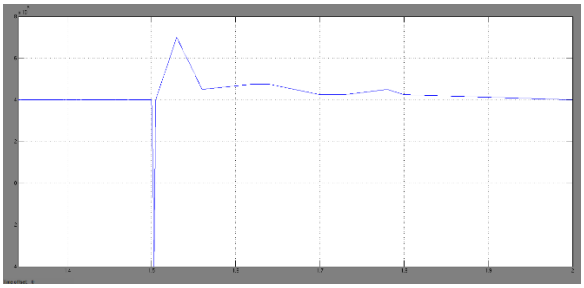
C. DC Fault Line Current Control Mode



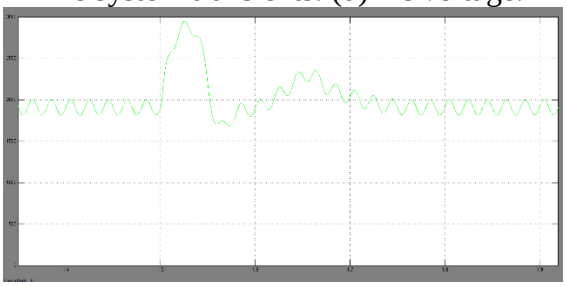
The system transients: (a) DC current



The system transients: (b) arm current



The system transients: (d) Dc voltage.



The system transients: (d) capacitor voltages.

Fig. 11 The system transients: (a) DC current, (b) arm current, (c) DC voltage, and (d) capacitor voltages.

D. Pole-to-Ground Fault in Bipolar HVDC Grid

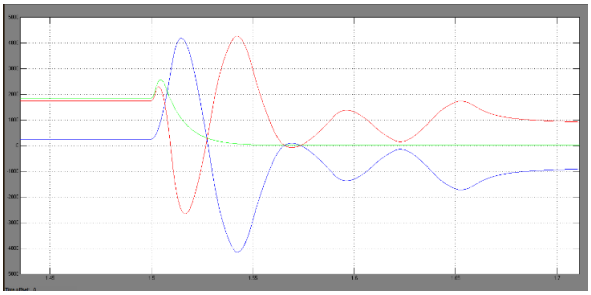
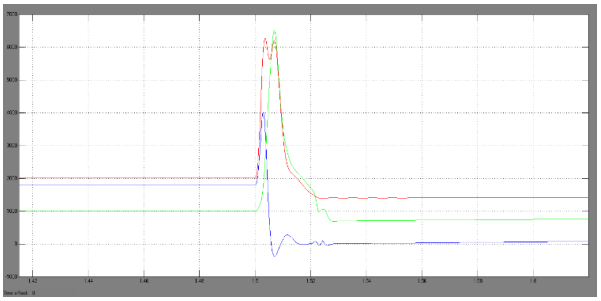


Fig. 12 The DC fault currents under PTG fault.

E. Coordinated Control of the HVDC Grid



Coordinated control results: (a) fault current

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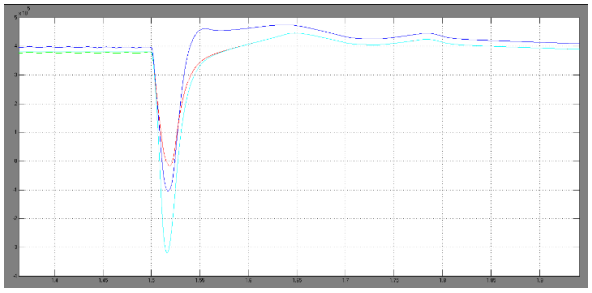
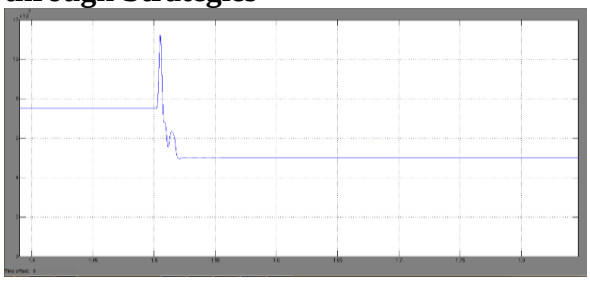


Coordinated control results: (b) DC voltage.

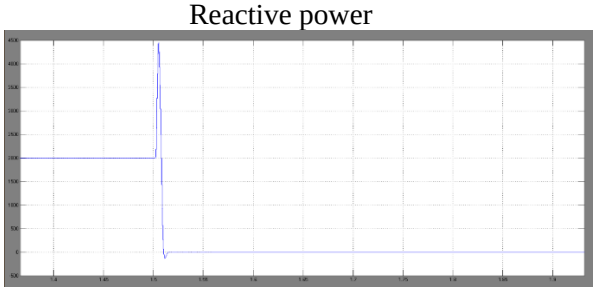
Fig. 13 Coordinated control results: (a) fault current and (b) DC voltage.

Simulation results with FLC:

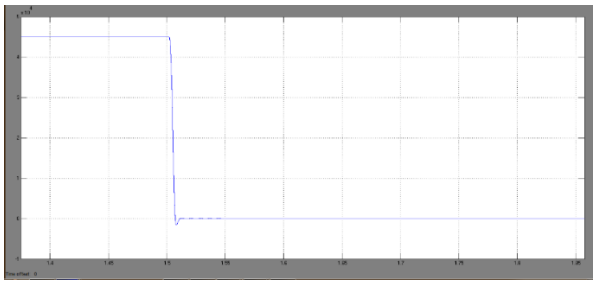
A. Comparison of Control Capability of Non-blocking and Blocking-based Ride-through Strategies



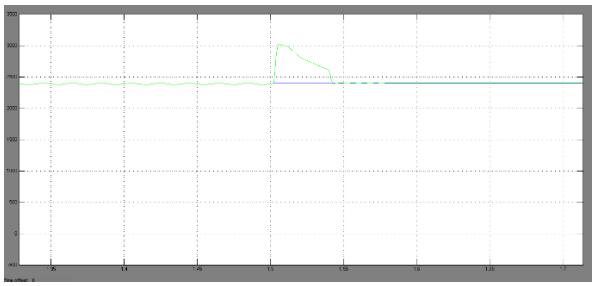
Reactive power



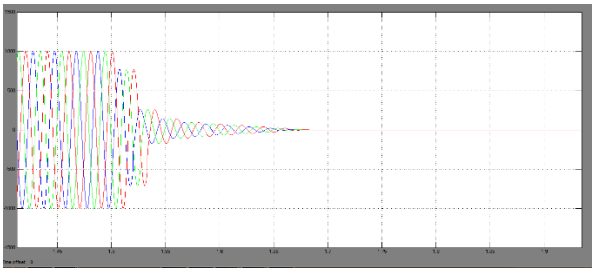
I1



Udc1

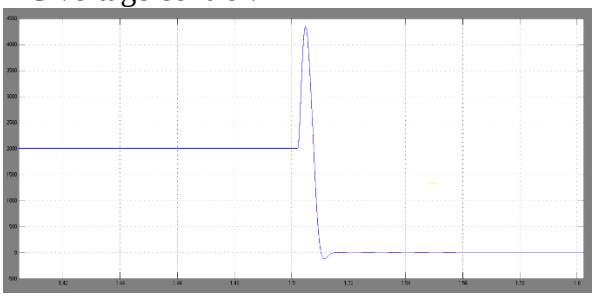


Sub module voltages

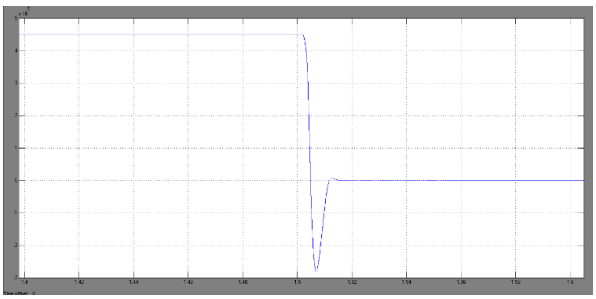


Upper arm current

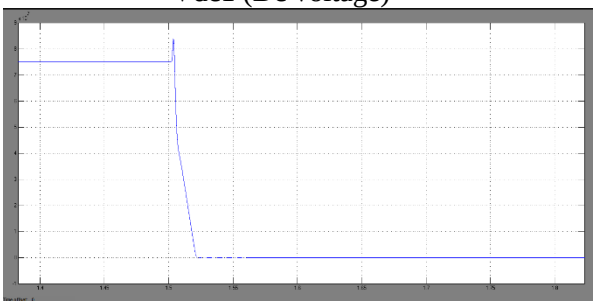
Fig. 14 Comparison of reactive power and DC voltage control:



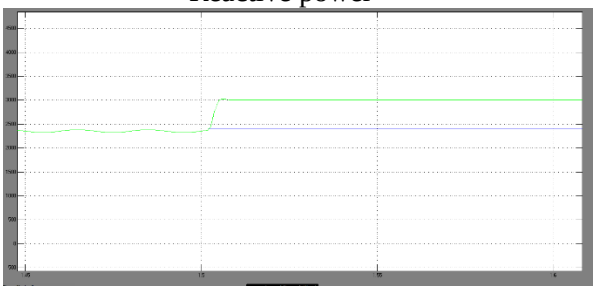
I1



Vdc1 (Dc voltage)



Reactive power



Sub module voltages

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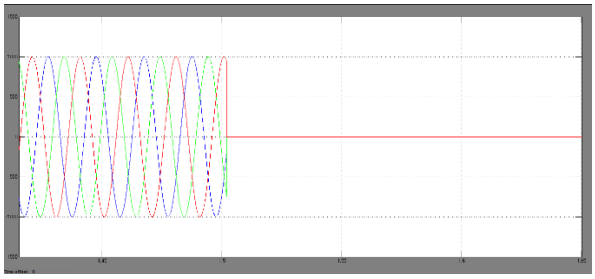
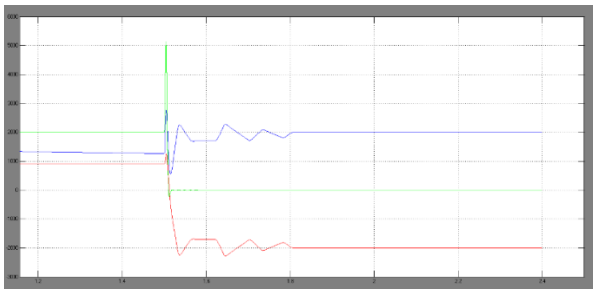


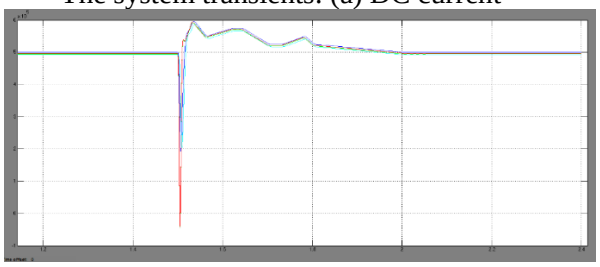
Upper arm current

Fig. 15 Comparison of reactive power and DC voltage control: (b) DC fault blocking-based ride through.

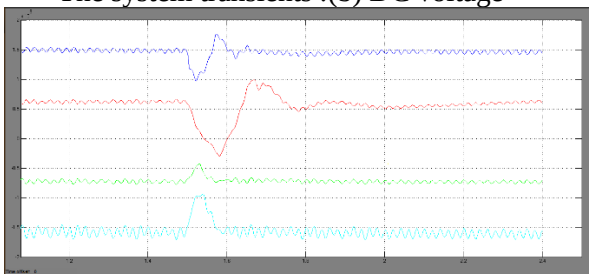
B. Converter DC Current Control Mode



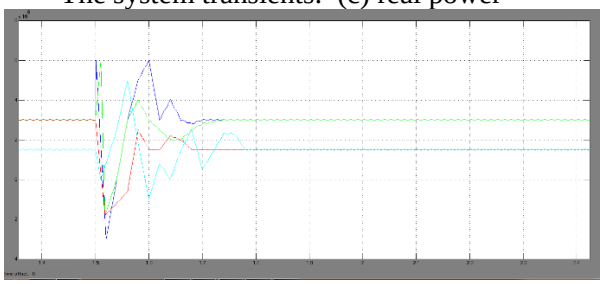
The system transients: (a) DC current



The system transients :(b) DC voltage



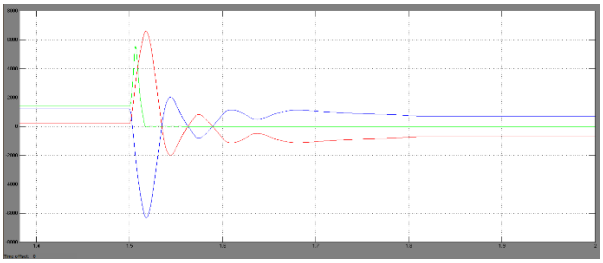
The system transients: (c) real power



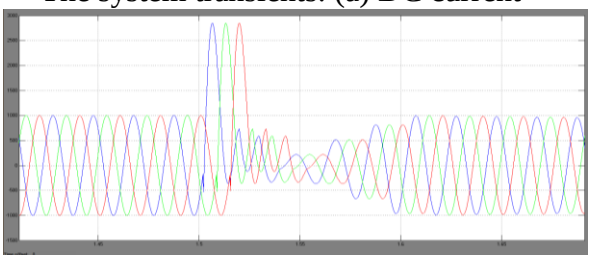
The system transients: (d) reactive power.

Fig. 16 The system transients: (a) DC current, (b) DC voltage, (c) real power, and (d) reactive power.

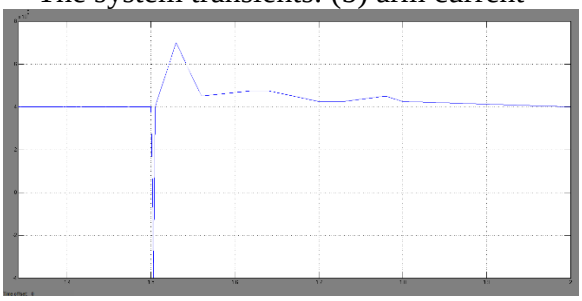
C. DC Fault Line Current Control Mode



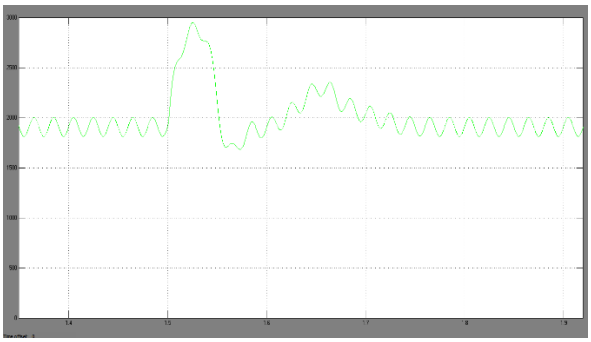
The system transients: (a) DC current



The system transients: (b) arm current



The system transients: (d) Dc voltage.



The system transients: (d) capacitor voltages.

Fig. 17 The system transients: (a) DC current, (b) arm current, (c) DC voltage, and (d) capacitor voltages.

D. Pole-to-Ground Fault in Bipolar HVDC Grid

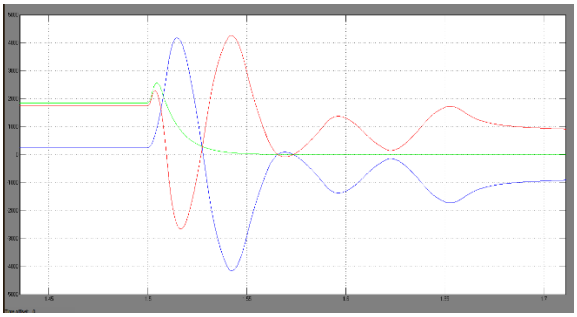
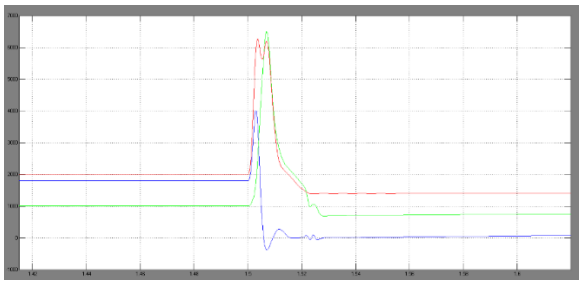
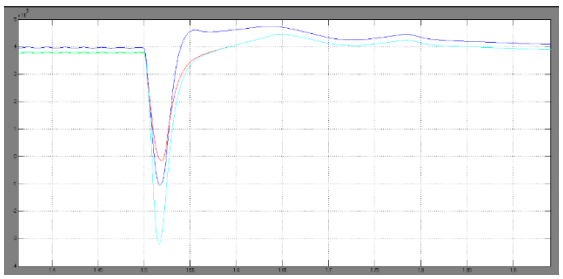


Fig. 18 The DC fault currents under PTG fault.

E. Coordinated Control of the HVDC Grid



Coordinated control results: (a) fault current



Coordinated control results: (b) DC voltage.

Fig. 19 Coordinated control results: (a) fault current and (b) DC voltage.

VII. CONCLUSIONS

This paper proposes a source-side essential and reinforcement flaw leeway plan of HVDC framework utilizing mixture MMC. The deficiency current advancement system is uncovered by checking the exactness of the mathematical outcomes looking at over the EMT reproductions. At that point the essential control squares of the mixture MMC which incorporates converter DC current control and DC separation point current control are given. The control plans are approved with PTP and PTG hamper, the control goals are accomplished and the HVDC framework can recuperate to a consistent state after the flaw cleared. The methodology is likewise contrasted and the valve obstructing based FRT system and demonstrated that the receptive force pay and DC voltage are just controllable in the non-impeding FRT procedure. In the proposed approach, the DCCBs are not needed which benefits the development of HVDC matrices. Exhaustive examination is led regarding constant force accessibility, shortcoming recuperation speed, proportion of the FBSM tally and gadget current security edge. The proposed control strategies for crossover MMC are similarly appropriate to HVDC matrices with even monopole and bipolar setup, coincided and spiral DC lattices.

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